What is claimed is:

1. A direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source supplying a current to the summing node and being connected to a power supply voltage, wherein the current at the summing node is equal to zero when the power supply voltage is equal to a preselected voltage; and

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to voltage changes in the summing node.

2. The direct current sum bandgap voltage comparator of claim 1, wherein the current sources supply currents according to a band-gap equation.

3. The direct current sum bandgap voltage comparator of claim 2, wherein the band-gap equation is:

$$K_1 (V_{CC} - V_T) + K_1 V_T = K_2 V_{BE} + K_3 (kT/q)$$

where V_{CC} is the power supply voltage, V_T is the threshold voltage, V_{BE} is the base emitter voltage, and kT/q is equal to the threshold voltage, V_T, where k is Boltzman's constant, T is the temperature in kelvin, q is the electronic charge, and K_1, K_2, and K_3 are constants.

4. The direct current sum bandgap voltage comparator of claim 3, wherein the plurality of current mirrors comprises four current mirrors.

5. The direct current sum bandgap voltage comparator of claim 4, wherein the first current mirror includes a plurality of transistors and supplies a current to the summing node defined by $K_1(V_{CC}-V_T)$, where V_{CC} is the power supply voltage and V_T is a threshold voltage in the first current mirror.

6. The direct current sum bandgap voltage comparator of claim 5, wherein the second current mirror includes a plurality of transistors and supplies a current to the summing node defined by K_1V_T, where V_T is a threshold voltage in the second current mirror.

7. The direct current sum bandgap voltage comparator of claim 6, wherein the third current mirror includes a plurality of transistors and supplies a current to the summing node defined by K_2V_{BE}, where V_{BE} is a base-emitter voltage defined by a selected transistor in the third current mirror.

8. The direct current sum bandgap voltage comparator of claim 7, wherein the fourth current mirror supplies a current to the summing node defined by $K_3(kT/q)$.

9. The direct current sum bandgap voltage comparator of claim 8 further comprising a clamping circuit connected to the summing node, wherein a voltage swing, responsive to changes in current supplied by the current mirrors, may be selected for the summing node.

10. The direct current sum bandgap voltage comparator of claim 8 further comprising a cascode stage interposed between the summing node and the current mirrors.

11. The direct current sum bandgap voltage comparator of claim 8 further comprising a hysteresis circuit connected to the indicator circuit to reduce noise.

12. The direct current sum bandgap voltage comparator of claim 8, wherein the indicator circuit includes a pair of inverters connected in series, wherein an input in the first inverter is the input of the indicator circuit connected to the summing node and an output of the second inverter is the output of the indicator circuit.

13. The direct current sum bandgap voltage comparator of claim 12, wherein the indicator circuit provides a logic one output if the power supply is equal to or greater than a preselected voltage.

22. The zero power circuit of claim 21, wherein the fourth current mirror supplies a current to the summing node defined by $K_3(kT/q)$.

23. The zero power circuit of claim 22 further comprising a clamping circuit connected to the summing node, wherein a voltage swing, responsive to changes in current supplied by the current mirrors, may be selected for the summing node.

24. The zero power circuit of claim 22 further comprising a cascode stage interposed between the summing node and the current mirrors.

25. The zero power circuit of claim 22 further comprising a hysteresis circuit connected to the indicator circuit to reduce noise.

26. The direct current sum bandgap voltage comparator of claim 22, wherein the indicator circuit provides a logic one output if the power supply is equal to or greater than a preselected voltage.

14. A zero power circuit comprising:

a first circuit;

a direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source supplying a current to the summing node and being connected to a power supply voltage, wherein the current at the summing node is equal to zero when the power supply voltage is equal to a preselected voltage; and

an indicator circuit having an input connected to the summing node and generating a logical signal at an output, responsive to changes in the summing node; and

a switching circuit for providing power to the first circuit from a primary power supply and a secondary power supply, the switching circuit being connected to the output of the indicator circuit, wherein power from the primary power supply is supplied to the first circuit if the logical signal indicates that the power supply voltage is equal to or greater than the preselected voltage and power from the secondary power supply is supplied to the first circuit if the power supply voltage is less than the preselected voltage.

15. The zero power circuit of claim 14, wherein the current sources supply currents according to a band-gap equation.

16. The zero power supply circuit of claim 15, wherein the band-gap equation is:

$$K_1 (V_{CC}-V_T) + K_1 V_T = K_2 V_{BE} + K_3 (kT/q)$$

where V_{CC} is the power supply voltage, V_T is the threshold voltage, V_{BE} is the base emitter voltage, and kT/q is equal to the thermal voltage, where k is Boltzman's constant, T is the temperature in kelvin, q is the electronic charge, and K_1, K_2, and K_3, are constants.

17. The zero power circuit of claim 16, wherein the plurality of current mirrors comprises four current mirrors.

18. The zero power circuit of claim 16, wherein the secondary power supply is a battery.

19. The zero power circuit of claim 17, wherein the first current mirror includes a plurality of transistors and supplies a current to the summing node defined by $K_1(V_{CC}-V_T)$, where V_{CC} is the power supply voltage and V_T is a threshold voltage in the first current mirror.

20. The zero power circuit of claim 17, wherein the second current mirror includes a plurality of transistors and supplies a current to the summing node defined by K_1V_T, where V_T is a threshold voltage in the second current mirror.

21. The zero power circuit of claim 20, wherein the third current mirror includes a plurality of transistors and supplies a current to the summing node defined by K_2V_{BE}, where V_{BE} is a base-emitter voltage defined by a selected transistor in the third current mirror.